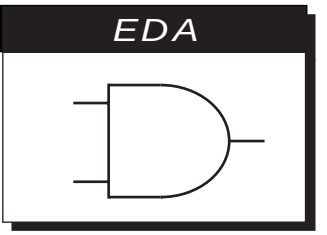

Spice uncovers regulator-stability problems

Steven M Sandler

An adjustable linear regulator, the LM317 is one of those products that seems to have been around forever. With it, engineers can provide local voltage regulation where one resistor sets the output voltage. Over the years several manufacturers have introduced many variations to cover applications that involve lower power, higher power, higher voltage and everything in between. The regulator is available in almost every conceivable package: surface mount, through hole, chassis mount and even as die for use in hybrids. Most people assume the device works just fine, but they've got problems they weren't even aware of. In particular, its stability isn't rock solid. To find out how much of a problem exists, this column shows how I analyzed the device with Spice in an effort to come up with a few solutions; alternatively you can measure the problem with a scope and find a circuit patch that comes close to the optimum solution.

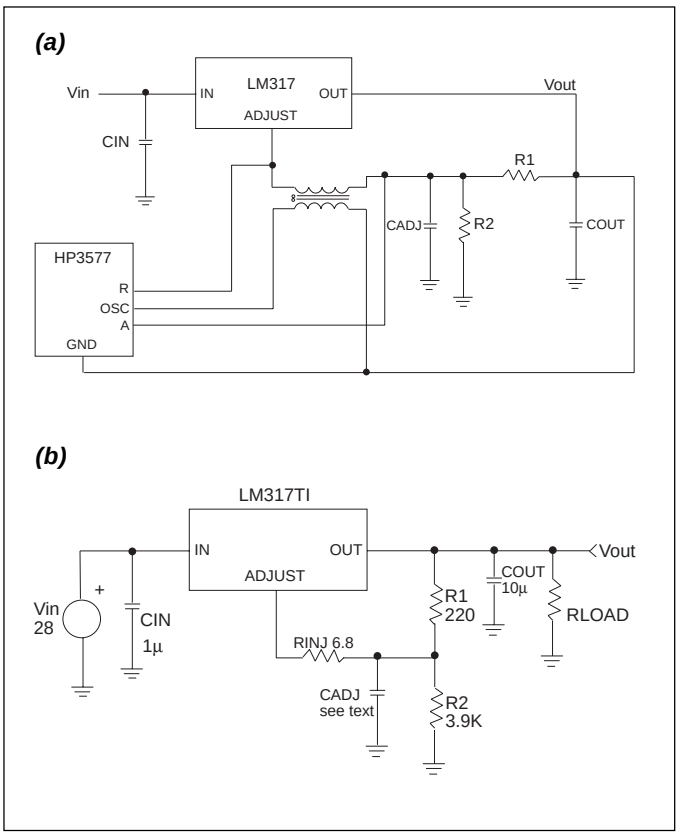

Fig 1—The test setup to measure the stability of the LM317 (a) uses a network analyzer to measure the device's open-loop gain and phase response. The schematic of the test circuit for Spice simulation of the setup uses a 6.8Ω resistor to model the effect of the network analyzer (b). Listing 1 gives the Spice code for the LM317 model.

The problem

In putting together several applications recently, I had reason to analyze this regulator's stability. Interestingly, manufacturers publish very little information concerning this aspect. App notes state that the device is stable for most values of load capacitance. They recommend a 1-µF tantalum or 25-µF aluminum electrolytic capacitor on the output to swamp out stability issues, while one manufacturer states that additional output capacitance further improves stability.

In general, suppliers recommend adding a 10-µF tantalum or electrolytic cap to bypass the adjustment pin to ground to improve ripple rejection and transient response—in other words, to improve stability. I have yet to see a Bode plot in any of the data I've reviewed, so how does an engineer go about analyzing the device's stability?

I began my own assessment by measuring the open-loop gain and phase response by generating Bode plots and also evaluating the transient-pulse load response in several applications. Then I correlated the

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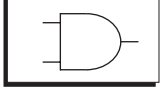

Listing 1

```
.SUBCKT LM317TI 1      2A    3
*CONNECTIONS  INPUT  ADJ. OUTPUT
*LM317 VOLTAGE REGULATOR - TI
VFIX 2A 2 .04
J1 1 3 4 JN
Q2 5 5 6 QPL .1
Q3 5 8 9 QNL  .2
Q4 8 5 7 QPL .1
Q5 81 8 3 QNL .2
Q6 3 81 10 QPL .2
Q7 12 81 13 QNL  .2
Q8 10 5 11 QPL  .2
Q9 14 12 10 QPL .2
Q10 16 5 17 QPL  .2
Q11 16 14 15 QNL .2
Q12 3 20 16 QPL .2
Q13 1 19 20 QNL .2
Q14 19 5 18 QPL .2
Q15 3 21 19 QPL .2
Q16 21 22 16 QPL .2
Q17 21 3 24 QNL  .2
Q18 22 22 16 QPL .2
Q19 22 3 241 QNL 2
Q20 3 25 16 QPL .2
Q21 25 26 3 QNL .2
Q22A 35 35 1 QPL 2
Q22B 16 35 1 QPL 2
Q23 35 16 30 QNL  2
Q24A 27 40 29 QNL .2
Q24B 27 40 28 QNL .2
Q25 1 31 41 QNL 5
Q26 1 41 32 QNL 50
D1 3 4 DZ
D2 33 1 DZ
D3 29 34 DZ
R1 1 6 310
R2 1 7 310
R3 1 11 190
R4 1 17 82
R5 1 18 5.6K
R6 4 8 100K
R7 8 81 130
R8 10 12 12.4K
R9 9 3 180
R10 13 3 4.1K
R11 14 3 5.8K
R12 15 3 72
R13 20 3 5.1K
R14 2 24 12K
R15 24 241 2.4K
R16 16 25 6.7K
R17 16 40 12K
R18 30 41 130
R19 16 31 370
R20 26 27 13K
R21 27 40 400
R22 3 41 160
R23 33 34 18K
R24 28 29 160
R25 28 32 3
R26 32 3 .1
C1 21 3 30PF
C2 21 2 30PF
C3 25 26 5PF
CBS1 5 3 2PF
CBS2 35 3 1PF
CBS3 22 3 1PF
.MODEL JN NJF(BETA=1E-4 VTO=-7)
.MODEL DZ D(BV=6.3)
.MODEL QNL NPN(EG=1.22 BF=80
RB=100 CCS=1.5PF TF=.3NS TR=6NS
CJE=2PF
+ CJC=1PF VAF=100)
.MODEL QPL PNP(BF=40 RB=20 TF=.6NS
TR=10NS CJE=1.5PF CJC=1PF VAF=50)
.ENDS
```

measured results to a Spice model of the circuit to estimate tolerances.

Measuring it

The first task was developing a test configuration to generate the Bode plots. It took a while finding a method of measuring loop gain because the internal reference, and therefore the

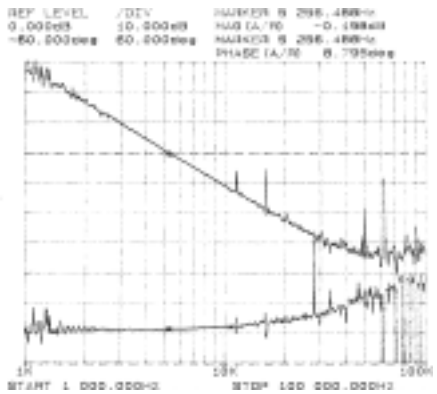

Fig 2—The Bode plot of test circuit with C_{adj} = 0 and R_{load} = 2.2 kΩ demonstrate the 317's poor phase margin.

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feedback signal to the 317, floats at the output voltage. Fig 1a shows a simple setup including an HP3577 network analyzer, while Fig 1b gives the schematic of the matching test circuit for simulation in Spice based on Listing 1.

The HP3577 plots the gain and phase of Ch A divided by Ch R. Note that the analyzer is floating on the regulator's output voltage. The 6.8Ω resistor, R_{inj}, has little effect on regulator stability but serves as the injection point for the network analyzer. When the analyzer isn't connected, I short out that resistor with a jumper.

Under test, regulator output measured 23.5V. I evaluated its stability with four values of R_{load} and three values of C_{adj} (Table 1). You can also find the Bode plot results for a 2.2-kΩ load resistor in Fig 2. Load current equals 10.7 mA plus an additional 5.7 mA for the current in the programming resistors (R_1 and R_2) for a total of 16.4 mA.

This circuit has a measured phase margin of 8.8°, which is poor for stability performance. A step/load response plot for this configuration

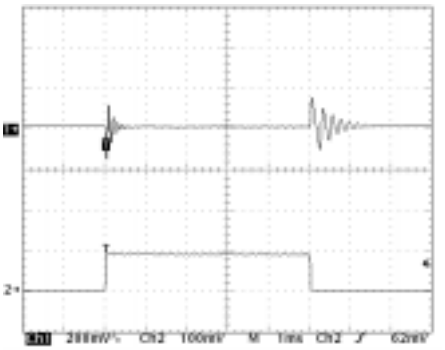

Fig 3—The transient response for 100 mA load step with C_{adj} = 0 and R_{load} = 2.2 kΩ exhibits a 5-kHz ringing (upper trace, V_{out} 200 mV/div; lower trace, load current 100 mA/div). Note that the ringing frequency is different on each edge of the step.

(Fig 3) confirms the poor phase margin. A MOSFET switch sets the load current, with the minimum amount flowing through a 2.2-kΩ resistor and with maximum current set by the MOSFET's gate voltage.

I draw three conclusions from this pulse-load response. First, based on the sustained ringing, it appears that the circuit exhibits poor phase margin. Second, at the lower current (with

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R_{load}	C_{adj}	Phase Margin	Bandwidth
(ohms)	(μF)	(deg)	(kHz)
2200	0	8.8	5.26
2200	0.0047	38.5	5.79
2200	10 (tantalum)	28.1	24.6
500	0	12.0	8.52
500	0.0047	60.3	10.8
500	10 (tantalum)	50.0	51.4
200	0	13.2	9.67
200	0.0047	64.9	13.2
200	10 (tantalum)	47.7	50.1
20	0	19.7	10.5

Table 1—A summary of the Bode plot results for various combinations of load resistor and adjustment capacitor show the large effect these two components have on phase margin and regulator bandwidth. Note that the bandwidth is a function of load and capacitance.

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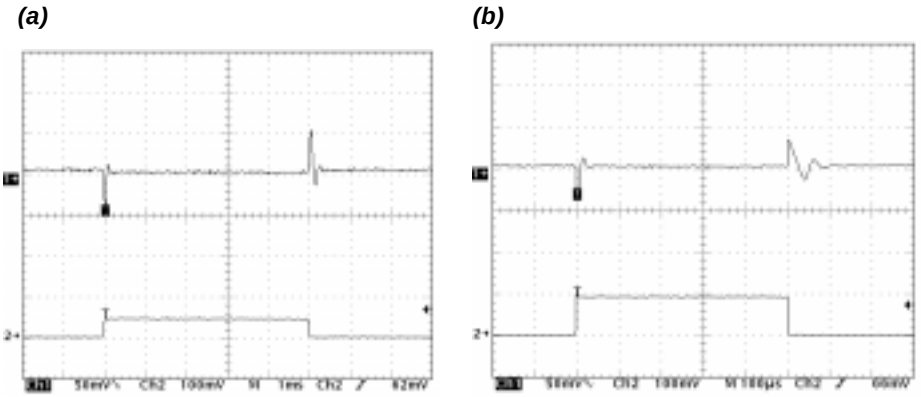

Fig 4—An improved transient response for a 100-mA step with C_{adj} = 0.0047 μF and R_{load} = 2.2 kΩ (a) shows significantly less ringing than Fig 3 (upper trace, V_{out} 200 mV/div; lower trace, load current 100 mA/div). The transient response for 100 mA step with C_{adj} = 10 μF and R_{load} = 2.2 kΩ (b) contains more pronounced ringing than in (a), indicating that adding capacitance past a certain point doesn't help (upper trace, V_{out} 200 mV/div; lower trace, load current 100 mA/div).

the 2.2-kΩ resistor), you can approximate the bandwidth from the 200-μsec ring period as 5 kHz, which agrees with the 5.2 kHz measured in Fig 2. Finally, at the two load currents that the pulse load represents, the ringing frequencies and thus the bandwidths are different.

The tabulated results in Table 1 show that stability is better with a 4700-pF capacitor than with either no adjustment cap or one at 10 μF, suggesting that the stability result is parabolic and an optimum value of capacitance exists. For the purpose of comparison, I repeated the step-load response with 0.0047-μF and 10-μF adjustment caps (Figs 4a and b). The ringing in the transient-response results confirm that a 0.0047-μF value yields a better phase margin than does a 10-μF cap.

As it turns out, the poor phase margin results from the internal dynamic resistance presented by the regulator's output transistors and the output capacitor. This dynamic resistance is certainly load dependent, but it's not a defined parameter, nor is the internal compensation—and thus it's difficult to predict or optimize stability. Those are aspects I'll address in my next column. ***PE&IN***

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Editorial Feedback
This article's value to me was:
High—272 Average—273 Low—274