Worst Case Circuit Analysis - An Overview (Electronic Parts/Circuits Tolerance Analysis)

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Key Words: Worst Case Analysis, Electronic Parts/Circuit Tolerance Analysis,Worst Case Scenario, Worst Case Part Variations, Sensitivity Analysis, Extreme Value Analysis, Root-Sum-Square, Monte Carlo Analysis.

SUMMARY & CONCLUSIONS

This paper has been prepared utilizing material from Design and Evaluation, Inc.'s (D&E) Training Course and Engineering Handbooks on Worst Case Circuit Analysis (WCCA). The WCCA Training Course was developed by D&E and upgraded under contract to NASA's Jet Propulsion Laboratory to standardize an approach to performing Worst Case Circuit Analysis and to exemplify the methodologies and tools for completing a customer acceptable Worst Case Circuit Analysis final report. The WCCA metholdologies discussed herein for the development of a Worst Case Parts Variation Data Base, Sensitivity Analysis and the mathematical approaches of the Extreme Value Analysis (EVA), Root-Sum-Square (RSS) and Monte Carlo Analysis for solving circuit equations and combining variables have become an accepted industry standard over the last eight years.

1. INTRODUCTION

The objective of this paper is to introduce the basic philosophy and concepts of Worst Case Circuit Analysis (WCCA) and to exemplify these principles.

The crux of this paper are the concepts of electronic piece-part parameters variations beyond their initial tolerance due to aging and environmental influences, the mathematical sensitivity of circuit performance to these variations, and the numerical methods, both non-statistical and statistical, of handling the numerous variables affecting circuit performance. The subjects of Sensitivity Analysis, and three mathematical techniques, namely Extreme Value Analysis, Root-Sum-Square and Monte Carlo Analysis are discussed herein.

The first questions to be addressed are "What is Worst Case Analysis ?" and "Why do it?" Figure 1.0 sums up the "What". The "Why" is three fold:

1 - To design reliability INTO hardware for long term trouble-free field operation - reliability against drift.

2 - WCCA is normally a contract requirement on most Hi-Rel Military and Space Programs.

3 - WCCA is "THE WAY" to design electronic circuits - given a Worst Case Part Variations data base, WCCA is relatively easy for circuit designers/analysts as well as an economical approach and if the circuit "passes" we're finished our job and should get through test easier than normal.

WORST CASE CIRCUIT ANALYSIS (WCCA) WHAT IT IS

- EVALUATION OF CIRCUITS FOR TOLERANCE TO DRIFT
  - A RIGOROUS MATHEMATICAL EVALUATION OF A CIRCUIT'S PERFORMANCE ATTRIBUTES AGAINST PERFORMANCE TOLERANCE LIMITS, UNDER **SIMULTANEOUS** EXISTENCE OF **ALL** THE MOST UNFAVORABLE CONDITIONS BEING AT RELIABLE LIMITS
  - PART PARAMETER VARIATIONS - WORST CASE
  - ENVIRONMENTAL EXTREMES, TEMP. ETC.
  - INPUT POWER
  - INPUT STIMULI, UPPER/LOWER LIMITS
  - LOAD VARIATIONS AT EXTREMES
  - I/F INTERFERENCES AT MAXIMUMS
- EVALUATION OF PARTS
  - OVER STRESSES IN WORST CASE CONDITIONS
  - IMPROPER APPLICATIONS
- FORMAL DOCUMENT

FIGURE #1

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The next questions to be answered are "How does WCCA fit into a Reliability Program?", "What is the Value of WCCA?" and "What is the Return on Investment?" Figures 2 and 3 answer the first two questions

The "Return on Investment" is difficult to assess for analysis tasks especially if a mission is 100% successful. It is recognized that the success of the mission of a complex system such as a satellite or the Space Shuttle Program is truly due to the collective efforts of various teams of people and technical disciplines all working and coordinating efforts and resources over a long time, toward the common goal of "success". However, ROI for a Worst Case Circuit Analysis Program has been addressed within a major government agency for a space program involving the launching of a satellite to orbit a neighboring planet. This satellite has been operating successfully for several years. For this program, a WCCA program was conducted over a four year period, involving fifty five boxes, and at a cost of two and a half million dollars. This WCCA effort uncovered and corrected twenty two major discrepancies, and sixty overstress conditions of parts of which eight were corrected and the remaining were accepted as minor. Two digital units were proven inadequate and redesigned. The WCCA Program costs less than 1% of total program costs and averted numerous potential failures of three hundred million dollars of hardware. The results economically justified the cost.

2 - OVERVIEW OF WORST CASE CIRCUIT ANALYSIS

The basic approach to performing a WCCA on a schematic for an electronic board is to breakdown the circuit into simple functional block and perform a WCCA on each block. The analyst should first document a detailed description of each block. He must then develop the Worst Case variations of all critical parameters for all parts utilized in the circuit, to arrive at a Worst Case MAX and a Worst Case MIN for each part parameter. This subject will be addressed in a following section. The analyst must then establish the performance requirements for the critical circuit attributes for each block and show analytically whether the circuit attributes actual performance values either meet or "fails to meet" the requirements, utilizing the WC MAX and WC MIN Values discussed above. Finally, the analyst should

HOW WCCA FITS INTO A RELIABILITY PROGRAM

DESIGN OBJECTIVES OF ELECTRONICS FOR AERO/SPACEFLIGHT PROJECTS

1 - DESIGN PERFORMANCE MUST REMAIN WITHIN SPECIFIED TOLERANCE LIMITS OVER ENTIRE MISSION LIFE

(NO DRIFT FAILURES)

TOOL: WORST CASE CIRCUIT ANALYSIS (WCCA)

2 - ALL PIECE PARTS MUST SURVIVE THE MAX LEVELS OF STRESS IMPOSED ON THEM

(NO CATASTROPHIC FAILURES)

TOOL: ELECTRICAL STRESS/DERATING ANALYSIS

3 - ASSESS MISSION EFFECTS IF A FAILURE IS ENCOUNTERED

(ALLEVIATE ADVERSE EFFECTS)

TOOL: FAILURE MODES & EFFECTS ANALYSIS

4 - DESIGN MUST RECOVER FROM "LOGIC UPSETS" WHICH **WILL OCCUR** DUE TO TRANSIENT RADIATION IN SPACE

(FAULT TOLERANT CIRCUITS)

TOOL: SINGLE EVENT UPSET ANALYSIS

NOTE:

TO DEVOTE MOST OF ONE'S RESOURCES TO SEVERAL OF THESE AREAS, TO THE NEGLECT OF THE OTHERS, YIELDS A PRODUCT ASSURANCE VOID - HIGH PROJECT RISK!

FIGURE 2

VALUE OF WCCA

DESIGNS HIGH RELIABILITY INTO CIRCUITS PROVIDES MARGIN AGAINST WC DRIFT OF PARTS OVER LIFE AND MAS ENVIRONMENTS.

SHORT TERM "RETURN ON INVESTMENT"

- REDUCES NUMBER OF HARDWARE DESIGN ITERATIONS DURING DEVELOPMENT PHASE
- REDUCES TIME IN TEST
- REDUCES NUMBER OF "DESIGN CHANGE NOTICES" AFTER DRAWING RELEASE

LONG TERM "RETURN ON INVESTMENT"

- INCREASES PRODUCTION EFFICIENCY
- TROUBLE FREE FIELD OPERATION
- LONG LIFE
- CUSTOMER SATISFACTION AND CONFIDENCE

WCCA IS COST EFFECTIVE IN BOTH THE SHORT AND LONG RUN

FIGURE 3

show how all the functionally blocks "play together" to meet the overall unit (board) requirements in the Worst Case.

2.1 CLASSICAL EVALUATION OF A BAND-PASS FILTER (BPF)

To illustrate the performance and results of a WCCA, we will utilize an example of a real WCCA which was performed on the Band-Pass Filter shown in Figure 4. The amplifier gain at the center frequency (A_{f0}) will be the circuit attribute selected for analysis.

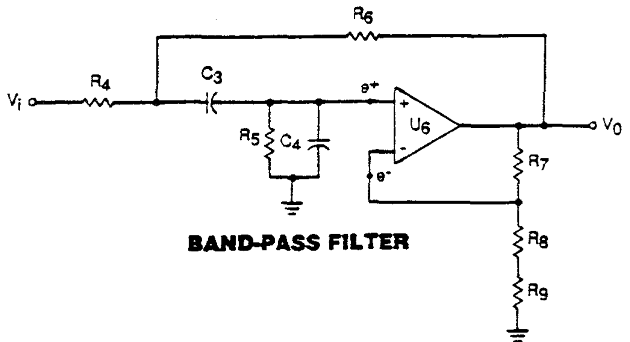


FIGURE 4

Given that U6 is an ideal OP-AMP ($R_{IN} = \infty$, $R_{OUT} = 0$, $A_{VOL} = \infty$), it does not enter into the equation for gain, which is

$$A_{f_0} = \frac{\dfrac{1}{R_1 C_2}}{\dfrac{R_5 + R_6}{R_4 + R_5 + R_6}\left[\dfrac{R_1 + R_3}{R_1 R_3}\left(\dfrac{1}{C_2} + \dfrac{1}{C_1}\right) + \dfrac{1}{R_2 C_2}\right] - \dfrac{1}{R_3 C_2}} \quad (1)$$

The specified requirement for the minimum A_{f0} is 7.0 VOLTS/ VOLT. The nominal and initial tolerance values for the resistors (R) and capacitors (C) are as follows:

C_1, C_2	= CYR20	(1500 pF, ±1%)
R_1, R_2, R_3	= RNR50	(15KΩ, ±1%),
R_4	= RNR50H	(40.2KΩ, ±1%)
R_5	= RNR50H	(10KΩ, ±1%),
R_6	= RNR50H	(1.21KΩ, ±1%)

Substituting the nominal part values into equation 1 yields A_{f0} = 11.08 V/V which shows the result to be "in spec". For a more pessimistic answer we could use the piece part initial tolerance values (± 1%) which would yield A_{f0} = 7.84 V/V, again "in-spec". It should be noted that the initial tolerance values for the R's and C's are the most pessimistic values which the analyst has available to him and this is how circuits are typically designed and analyzed.

BUT - will the circuit survive the real world environments to which it will be exposed during its mission, in the Worst Case? What is that were looking for.

2.2 CREATING A WORST CASE SCENARIO

Were looking to determine if there is any margin left in the circuit after we calculate the Worst Case MAX and Worst Case MIN performance and compare these values to the upper and lower tolerance limits which cannot be exceeded per the circuit design specifications, see Figure 5.

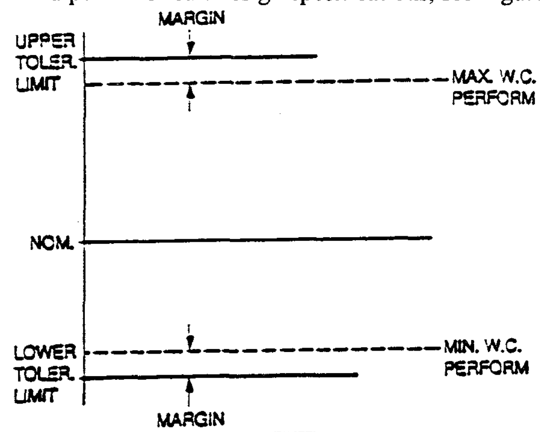


FIGURE 5

Normally, the Worst Case calculations must be performed twice i.e. to assess WC performance against the upper and lower spec limits. For the Band Pass Filter we have a one sided requirement i.e. the minimum gain is all we are interested in. We cannot go below the required minimum gain of 7.0 V/V in the Worst Case.

2.2.1 THE WORST CASE, PART VARIATIONS, DATA BASE (WCDB)

Two facts of life: first, when a part vendor specifies an initial tolerance (procurement tolerance), he is merely guaranteeing that when you buy the part and when you receive it in-house, that all the parts in each lot will fall within the initial tolerance specified (± 1% for the R's and C's of the Band Pass Filter). He is NOT guaranteeing that the part will remain within this tolerance band forever. Fact #2, the part will drift beyond the value it has, after you select it from stock and power it up and expose it to the limits of all the mission environments. In many, many, cases, especially those involving long missions, the part will drift beyond its initial tolerance, which we used in designing the circuit. Worst Case Analysis philosophy stacks up each maximum possible drift value contributed by each mission environment, i.e. they are added algebraically to the initial tolerance. See Figure 6.

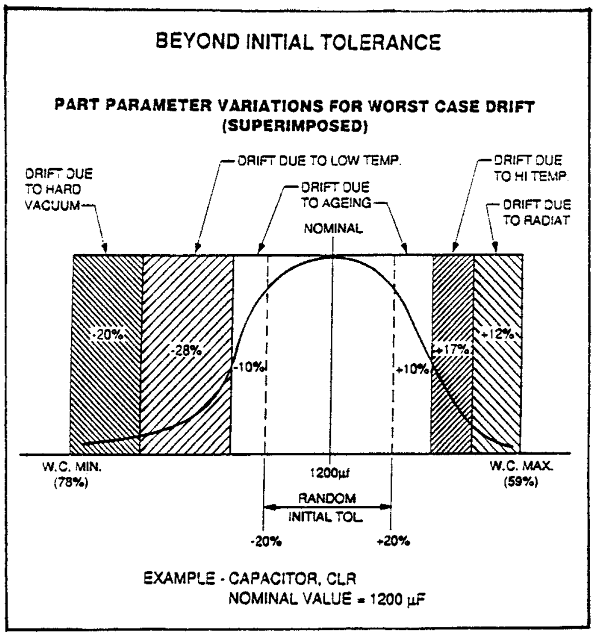


FIGURE 6

PART PARAMETER VARIATIONS
INITIAL TOLERANCE VS WORST CASE LIMITS
(ACTUAL DATA FROM DATA BASE 8K - SATELLITE PROG.)

	INITIAL TOL.	WORST CASE LIMITS (%) (MIN)	(MAX)
CAPACITOR CKR06, 1.0 µf	±20%	-53.1	+38.7
CAPACITOR, 10,000 pf	±5%	-10.3	+10.5
CAPACITOR CSR	±5%	-12.4	+15.4
CAPACITOR FIXED ELEC., 1200 µf	±20%	-44.5	+34.5
CAPACITOR TANT. NON-SOLID, 1200 µf	±20%	-38.5	+42.0
RESISTOR, RNN 1/8 W	±1%	-1.27	+1.48
RESISTOR, RWR 2 W	±1%	-1.14	+1.55
RESISTOR, NETWK PREC WW	±2.5%	-2.5	+5.50
RESISTOR, CC 1/4 W RCR	±5%	-17.6	+12.4
RESISTOR, CC 1/2 W RCR 20	±5%	-16.4	+10.3
XFMR, PULSE (INDUCTANCE)	±25%	-48.3	+38.2
XFMR, CURR, SHARING (INDUCTANCE)	±23%	-46.4	+36.3
INDUCTOR, LINEAR (INDUCTANCE)	±12.2%	-38.2	+16.2
DIODE, FET CURR. REG (ID)	±5%	-27.9	+32.6
DIODE, Z, VZO	±5%	-9.6	+7.7
DIODE, FAST REC (VFO)	±25%	-44.7	+41.9

FIGURE 7

For Worst Case Circuit Analysis, it is assumed that when you select a part from stock, it is at its initial tolerance value already, which it may or may not be but it is certainly possible and we are creating a Worst Case Scenario. Next we assume for WCCA, that all parts in a circuit are at their max drift values (on top of initial tolerance). SIMULTANEOUSLY. Now, admittedly, this is stretching things but it is a possible scenario in the worst case. A more likely scenario, is that some combinations of parts will be at drift values beyond their initial tolerance and probably they will not all be at the maximums possible drift. Survival in a worst case scenario of all parts being at their MAX drift values simultaneously, assures survival in any scenario of possible combinations of part variations to any degree. If you analytically calculate circuit performance under the Worst Case Scenario described above and still have margin in your circuit relative to not exceeding the specified upper and lower performance tolerance limits, you will have a rock solid design against part variations. This is the philosophy of Worst Case Circuit Analysis and this is how electronic circuits and systems are designed for most military and aerospace applications requiring high reliability.

WORST CASE CIRCUIT ANALYSIS DESIGNS RELIABILITY INTO ELECTRONIC CIRCUITS.

Figure 7 shows a comparison of some typical piece part initial tolerance values vs. the Worst Case limits. This table was compiled from an actual Worst Case Data Base for a major commercial satellite program. The Worst Case limits shown were used in the actual designs of the satellite which has been operating successfully for approximately five years with five to go to complete its mission.

The actual task of developing the Worst Case Parts Data Base is a significant part of the work and cost involved in performing a Worst Case Circuit Analysis. The goal of this task is to develop a document consisting of Worst Case Data Base (WCDB) Worksheets, as shown in Figure 8, for all electronic parts utilized on a program. There worksheets must be filled out by an engineer experienced with electronic parts. These worksheets, serve as a quantitative assessment of the dominant sources of variability for each part type for the environments and life of the program mission.

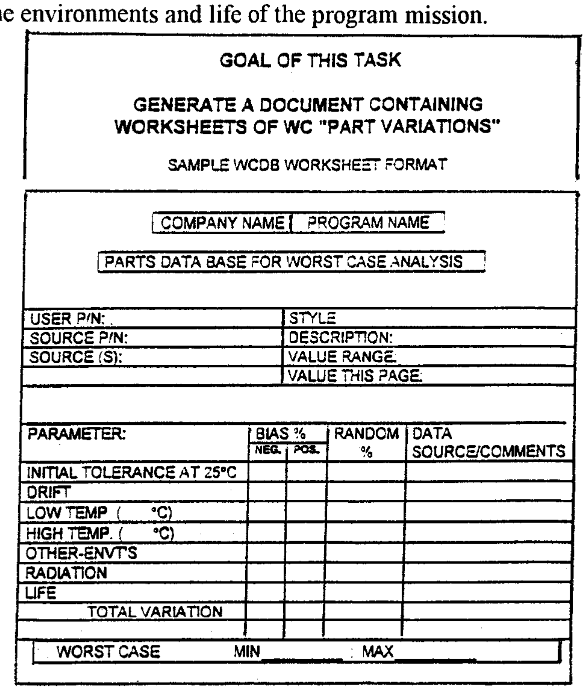


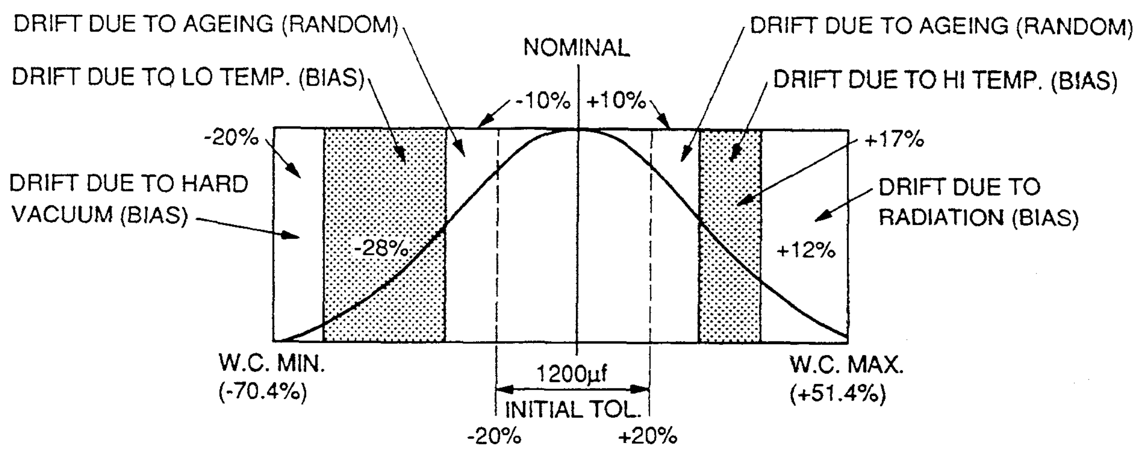
FIGURE 8

The Worst Case Data Base will serve as a program uniform reference source to assure that all Worst Case Circuit Analyses performed on the program (and there are many on large programs) utilize identical source data. You do not want all design engineers on a program developing their own W.C. Data Base. Once developed within a company, the Worst Case Data Base can be maintained, expanded and tailored for usage on other programs. The "how to develop" aspects of a Worst Case Data Base takes approximately four hours in the WCCA Training Course mentioned in the Summary at the beginning of this paper and hence is far beyond the scope of this paper which is only a brief overview of a complex task. At this point the reader should simply understand what the Worst Case Date Base is and the paramount need for its development and availability to all design engineers and analysts on a program who are involved with Worst Case Circuit Analysis.

versa. It's predictable. A random variation is totally unpredictable in which way the part value changes regardless of which direction the environment changes. These bias and random variations can be different for different part types, e.g. a particular environment change may cause a bias change of one part parameter type but a random change for another. Some drift effects may even be a combination of bias and random variations (e.g. Temp. Coef. = 100 ± 10 PPM/°C).

The question being posed is "How do we combine Bias and Random Variations to arrive at the WC MAX and the WC MIN part parameter values. One acceptable method, and the recommended method unless dictated otherwise, on numerous military programs is as shown in equations 2 and 3 i.e. add biases algebraically and Root-Sum-Square (RSS) the random variations. RSS is a statistically correct manner to

STATISTICS OF PART VARIATIONS



EXAMPLE: CAPACITOR, CLR
NOMINAL VALUE = 1200µf

FIGURE 9

One final important consideration in the development of a Worst Case Data Base which the reader should be aware of, is the manner in which we can statistically combine the individualized part variations (temp., life, radiation etc.), once the drift limits have been determined, to arrive at the WC MAX and WC MIN for the parameters. Looking of Figure 8, notice that there are columns for entering the variations due to the environments as either a "BIAS" variation or a "RANDOM" variation. The manner in which these variations are combined becomes a program choice if not dictated by the customer, and it does indeed make a difference. Figure 9 above illustrates examples of bias and random variations. A bias variation simply means that the parameter changes (increases or decreases) in the same direction as the environment changes (increases or decreases), e.g. if temperature increases, the part parameter value increases (positive temperature coefficient) and vice

combine random variables.

$$\text{W.C. MIN} = \text{NOMINAL VALUE} - \Sigma\ \text{NEG. BIASES} - \sqrt{\Sigma(\text{RANDOMS})^2} \quad (2)$$

$$\text{W.C. MAX} = \text{NOMINAL VALUE} + \Sigma\ \text{POS. BIASES} + \sqrt{\Sigma(\text{RANDOMS})^2} \quad (3)$$

Some agencies and prime contractors require that the random terms be treated as biases and hence added algebraically as shown in equation 4 and 5.

$$\text{W.C. MIN} = \text{NOMINAL} - \Sigma\ \text{NEG BIASES} - \Sigma\ \text{RANDOMS} \quad (4)$$

$$\text{W.C. MAX} = \text{NOMINAL} + \Sigma\ \text{POS. BIASES} + \Sigma\ \text{RANDOMS} \quad (5)$$

This method creates a worst, worst case scenario and is known as the Extreme Value Method (EVA) for combining part variations. Later, we will also discuss EVA and RSS analysis of circuits for WCCA.

2.2.2 OTHER CONTRIBUTING FACTORS TO A WORST CASE SCENARIO

Additional factors contributing to a Worst Case Scenario which must be taken into account are the interface connections, i.e. the box/circuit input power, input signals and loads, all of which have specified tolerance limits around the nominal values. In performing a WCCA, all these interface values must be set to their limit and in the direction (±) which causes the biggest problem for the circuit attribute under analysis.

2.3 SENSITIVITY ANALYSIS

Referring back to equation #1 for the gain of the Band-Pass Filter, we stated that substituting the nominal part values for all the R's and C's into equation #1 would yield a gain of 11.08 V/V and that substituting the initial tolerance values for all the R's and C's into equation #1 would yield a gain of 7.84 V/V. Using nominal values, it was a straight forward substitution of the part values. However, using initial tolerance values, which have an algebraic sign (±) with each part value, we had to make a choice of either the "+" value or the "-" value for each part to drive the gain to a minimum. The problem arises as to what combination of the "parts" MAX and MIN values will yield the circuit parameter MAX and MIN values? We must determine the circuit sensitivity direction response (i.e. circuit value increases or decreases) for the directional change (+ or -) for each part. Worst Case Circuit Analysis requires performing this same circuit "Sensitivity Analysis" since we are dealing with part MAX and MIN values. This analysis is absolutely mandatory since one wrong sign for any part will totally void the Worst Case solution. The classical solution for determining the sign of the sensitivity for each part when solving for either the circuit parameter Worst Case MAX or Worst Case MIN is to take the partial derivative of the circuit equation with respect to each part individually. That will yield the "sign" of the part which must be used. For the Band-Pass Filter, the equation is

$$A_{f_0} = A_{f_0}(NOM) \pm \sum_{i=1}^{N} \frac{\partial A_{f_0}}{\partial P_i} (P_i - P_{i\text{-}NOM}) \qquad (6)$$

Fortunently, many circuit simulators allow one to perform this sensitivity analysis. If such a program is not immediately available, there are other means to determine sensitivity e.g. substitute small incremental changes in each part individually (holding all other part values constant) and solve the circuit equation to see in which direction it changes (increases or decreases). You could also sweep the gain over a fairly wide range of each part value and display these graphically as shown in figure 10.

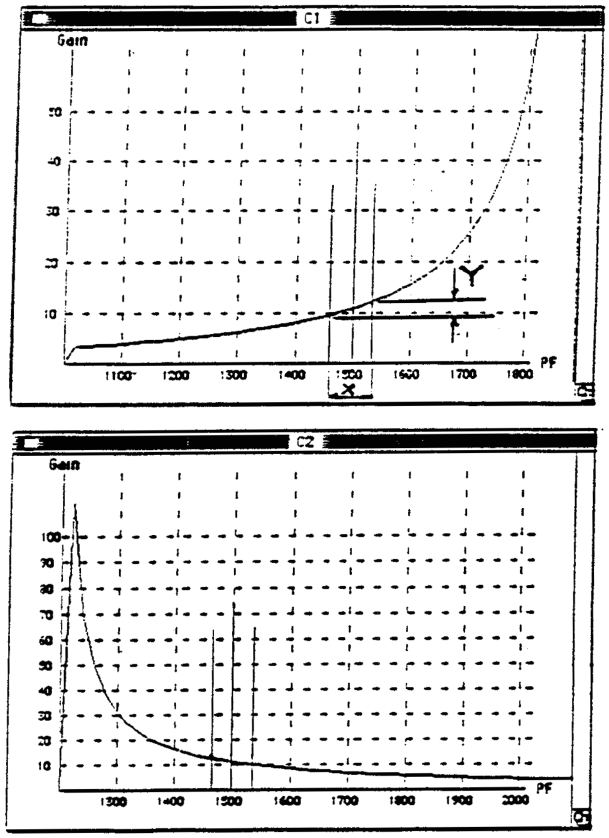


FIGURE 10

Notice in figure 10 that as C1 increases the circuit gain (A_{f0}) increases (positive sensitivity for C1) and as C2 increases the gain A_{f0} decreases (negative sensitivity for C2).

2.4 WORST CASE EVALUATION OF THE BAND-PASS FILTER

To evaluate the Worst Case minimum gain at the center frequency (A_{f0}) for the Band-Pass Filter (Figure 4 and equation 1), we need to determine the WC MAX and WC MIN for the R's and C's. This was done and is illustrated in figure 11.

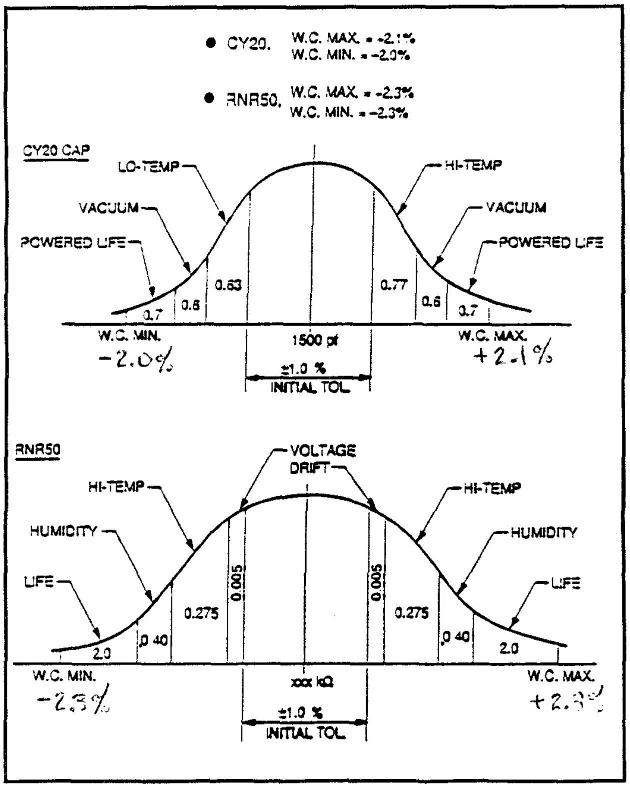


FIGURE 11

All variations were treated as biases. Note that Vi and Vo of Figure 4 do not enter into equation 1. If they did we would have to set them at their max or min tolerance also. We now must determine the directional (+ or -) sensitivity of each part. This was doing using a simulator which performed sensitivity analysis. See figure 12.

PIECE PART	SENSITIVITY $\left(\frac{\partial A_{f_i}}{\partial P_i}\right)$	PART VALUE FOR A_{f_0} MAX. (pf/Ω)	PART VALUE FOR A_{f_0} MIN. (pf/Ω)
C1, 1500 pf	+	1532	1470
C2, 1500 pf	-	1470	1532
R1, 15 KΩ	+	15.345	14.655
R2, 15 KΩ	+	15.345	14.655
R3, 15 KΩ	-	14.655	15.345
R4, 40.2 KΩ	+	41.125	39.275
R5, 10 KΩ	-	9770	10.230
R6, 1210 Ω	-	1182	1238

FIGURE 12

Substituting the WC MAX and MIN values into equation 1 for A_{f0} and in the proper direction dictated by the sensitivity analysis yields A_{f0} = 5.76 V/V which fails the minimum gain requirement of 7.0 V/V by quite a bit. The A_{f0}using all nominal or all initial tolerance values passed the requirement of 7.0 V/V. This was a real example from an actual WCCA. See figure 13.

Notice the significant difference between the nominal solution (11.08 V/V) and the initial tolerance (7.84 V/V) and the Worst Case (5.76 V/V) solutions.

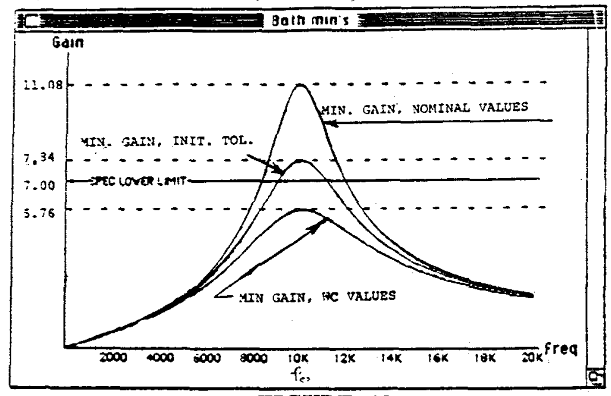


FIGURE 13

Note that we do not have to drive all the R's and C's to their Worst Case limits to cause A_{f0} to fall below 7.0 V/V, A_{f0} WC = 5.76 V/V. There are numerous combination of only several parts exceeding their initial tolerance which would cause the gain to fall below 7.0 V/V.

The circuit approach taken, i.e. substitution of piece-part WC MAX and WC MIN values into the circuit equation is called the Extreme Value Analysis (EVA). there are two other circuit techniques which can be utilized for a Worst Case Circuit Analysis. These are discussed briefly in the next section.

2.5 Alternate Techniques for performing Worst Case Circuit Analysis (WCCA)

Two alternate approaches for performing a WCCA will now be discussed. They are the ROOT-SUM-SQUARE (RSS) Analysis and the Monte Carlo Analysis (MCA). Both techniques are valid approaches. These two subjects consume about an hour and a half in the WCCA Training Course mentioned in the Summary and hence can be given only a brief treatment herein. Both techniques yield results which are more optimistic then the Extreme Value Analysis (EVA) solution. Discussion of both techniques herein use an example of a simple voltage divider circuit with four resistors, ($R_1 \rightarrow R_4$) and two internal voltages sources (V_1 and V_2). The equation for the output voltage is given in equation 7.

$$V_0 = \left[\frac{V_1 R_2}{R_1 + R_2} + V_2\right] \times \frac{R_4}{\frac{R_1 R_2}{R_1 + R_2} + R_3 + R_4} \tag{7}$$

ROOT-SUM-SQUARE (RSS)

RSS is the statistical technique for combining standard deviations (σ).

The RSS approach is based on the "Law of large numbers" (Central Limit Theorem) which states that if a large number of variables are statistically combined the resulting distribution is a normal distribution independent of the form of the distributions of the variables which are combined.

The determination of the standard deviation (σ) of a normal distribution for any circuit attribute by mathematically combining the standard deviations of each piece-part based on the magnitude of the sensitivity of the circuit attribute to the value of the piece-part is therefore a valid statistical approach.

The normal distribution of the output curve for Vo has a standard distribution related to the standard deviations of the part parameters as shown in equation 8.

The standard deviation of the output variable Vo will be identified as σ_T. Multiplying the solution of equation 8 by three will yield us the 3σ (99.7%) value for Vo which is herein defined as the Worst Case value.

$$\sigma_T = \sqrt{\left(\frac{\partial V_0}{\partial R_1}\sigma_{R1}\right)^2 + \left(\frac{\partial V_0}{\partial R_2}\sigma_{R2}\right)^2 + \left(\frac{\partial V_0}{\partial R_3}\sigma_{R3}\right)^2 + \left(\frac{\partial V_0}{\partial R_4}\sigma_{R4}\right)^2 + \left(\frac{\partial V_0}{\partial V_1}\sigma_{V1}\right)^2 + \left(\frac{\partial V_0}{\partial V_2}\sigma_{V2}\right)^2} \quad (8)$$

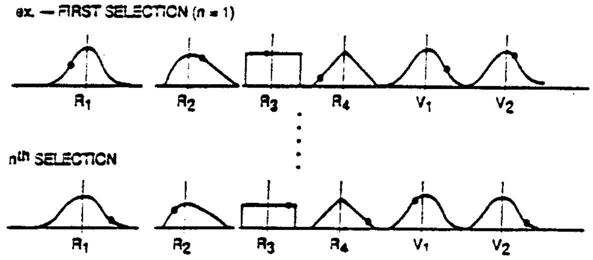
MONTE CARLO ANALYSIS (MCA)

The Monte Carlo Analysis is hereby defined as: The empirical determination of the statistical distribution of any circuit attribute by the repeated evaluation of that attribute under various circuit conditions in which the values of each piece-part are randomly selected.

The MCA process is illustrated in Figure 14.

MONTE CARLO ANALYSIS PROCESS

- REPEATEDLY SELECT RANDOM SETS OF VALUES. THIS PRODUCES A RANDOMLY CHOSEN REPLICA OF THE CIRCUIT FUNCTIONAL PERFORMANCE DISTRIBUTION



- CALCULATE V_0 FOR EACH SET VIA THE CIRCUIT EQUATION

$$V_0 = \left[\frac{V_1 R_2}{R_1 + R_2} + V_2\right] \times \frac{R_4}{\frac{R_1 R_2}{R_1 + R_2} + R_3 + R_4}$$

- REPEAT "n" TIMES (n >> # PARAMETERS)
- SORT AND GROUP RESULTS
- GENERATE V_0 HISTOGRAM OF FREQUENCY DISTRIBUTION

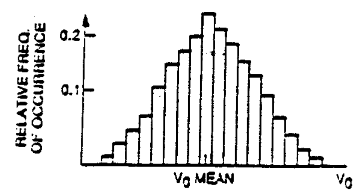


FIGURE 14

From the area of a histogram, one can now calculate the circuit Mean and Standard Deviation (σ). The 3σ (99.7%) value is again defined as the Worst Case Value. Fortunently, there are numerous simulators available which perform a Monte Carlo Analysis

CONCLUSIONS

Electronic production hardware requiring reliable operation over a period of time should never be built based on circuits which were designed utilizing only the nominal or initial tolerance values of the piece parts. Part values will drift over the life and environments of a mission after being assembled onto circuit boards. Worst Case Circuit Analysis is not a major deviation from the classical circuit design/analysis which electronic engineers normally perform in their daily work, given that the Worst Case Part Variations are developed or made available to the designer. In general, the required information to develop a Worst Case Parts Data Base (analytically) is available or can be extrapolated or estimated with rationale.

Worst Case Circuit Analysis on electronic circuits and systems has been performed for many years and the approach and analysis methods described herein have been acceptable to government agencies and major prime contractors.

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