A SPICE Macromodel for an Adjustable Positive Voltage Regulator

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ABSTRACT: *A macromodel has been developed for the LM117 Adjustable Positive Voltage Regulator. This model predicts AC, DC, Transient and Power-Up responses. Design formulas are presented for finding the component values of the macromodel which are based on pin measurements. The methodology of development is presented along with the experimental and simulated results.*

Introduction

The macromodel of an analog IC is a behavior model which uses an electronic equivalent circuit. This equivalent circuit is much simpler than the transistor level representation of the IC and approximately characterizes the DC, AC and Transient responses.

Macromodeling the AC Specifications

The functional block diagram for the LM117 is shown in Fig. 1. It is important in designing a macromodel that the components connected to the pins of the model are the same as those connected to the pins of the chip. This will help mimic the nonlinearities seen by loads. The LM117 has a Darlington pair for the pass transistor. Since this effectively increases β, then we can simplify this with a single transistor and lump the additional gain in the amplifier stage of Fig. 1.

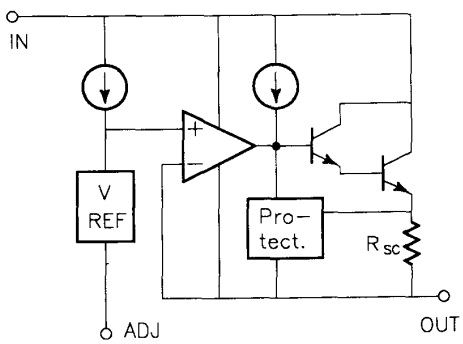

Figure 1. LM117 functional block diagram

In measuring the ripple rejection angle versus frequency it was found that the phase angle shifts from 0° up to 140° and back to 0° as the frequency is swept from low to high. This indicates a second order system. In addition, the measurements of the output impedance angle versus frequency yielded phase shifts from 0° to 80° and back to 0°. This seems to indicate a first order system or a second order system with a pole-zero cancellation.

Op-amps need a dominant pole for stability when used in feedback circuits. Since this is the case in the regulator, this gives us a first order circuit. The second pole or zero is probably due to the large pass transistor. A series RC across the collector-base will give a pole-zero to our system making it second order. This is shown in Fig. 2 where the amplifier has a zero at $1/(2\pi R_Z C_{PZ})$ and an approximate pole at $1/(2\pi R_P C_{PZ})$.

Our next task is to determine the formulas which govern this circuit. The regulator must be used in a feedback circuit in order to operate. Perhaps the best circuit to start with is the ripple rejection circuit. This is shown in Fig. 3a. Since there are eleven ac components plus the pass transistor components, then the task of analyzing this circuit by hand is tedious. There is a Symbolic-SPICE (Sspice) program, currently available, which will help find the AC response.

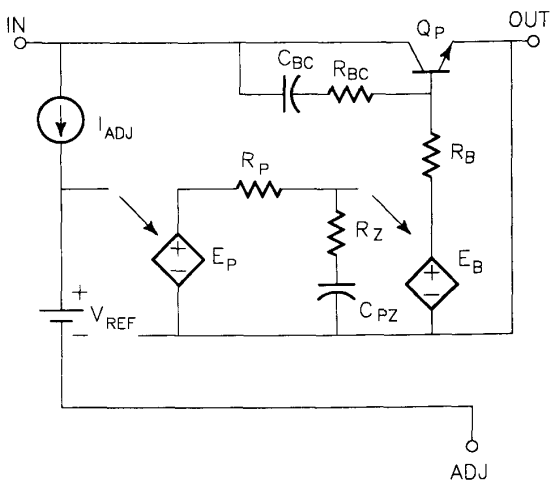

Figure 2. First pass macromodel

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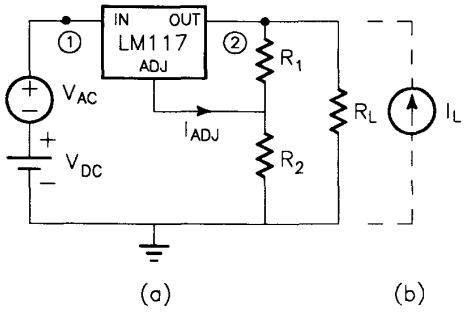


Figure 3. a) Ripple rejection b) Output impedance test circuits.

Using Sspice, we can find the expression for ripple rejection at low frequencies:

$$rr_{LF} = 1 + \frac{R_{OE}}{R_L} + \frac{R_{OE}}{R_1+R_2} + R_{OE}\frac{R_1}{R_1+R_2}\frac{\beta A_P}{R_B+R_\pi} \quad (1)$$

Since the open loop gain of the op-amp at low frequencies, A_P, and the β of the transistor are both large numbers, then Eqn. 1 is approximately the last term.

$$rr_{LF} \approx R_{OE}\frac{R_1}{R_1+R_2}\frac{\beta A_P}{R_B+R_\pi} \quad (2)$$

The other test circuit of interest is the output impedance. This circuit is shown in Fig. 3b. Again using Sspice, the low frequency output impedance is:

$$Z_{OUTLF} = (R_1+R_2) \parallel R_L \parallel R_{OE} \parallel \frac{R_\pi+R_B}{\beta A_P}\frac{R_1+R_2}{R_1} \quad (3)$$

Since the open loop gain of the op-amp at low frequencies, A_P, and the β of the transistor are both large numbers, then Eqn. 3 is approximately the last term

$$Z_{OUTLF} \approx \frac{R_\pi+R_B}{\beta A_P}\frac{R_1+R_2}{R_1} \quad (4)$$

Taking the product of Eqns. 2 and 4, we find that

$$rr_{LF} \cdot Z_{OUTLF} = R_{OE} = \frac{V_{AF}}{I_C} \approx \frac{V_{AF}}{I_L} \quad (5)$$

This gives us a macromodel parameter in terms of two measurements. With a low frequency *rr* of 69.7dB, which equals 3055, and a low frequency R_{OUT} of 0.050Ω both for a measured I_L = 0.2A, then R_{OE} = 152.75Ω and V_{AF} = 30.55.

The values of R_{OE} and R_π increase as I_L decreases. The measured value of the *rr* appears constant as I_L decreases. This indicates that in Eqn. 2, R_B+R_π is approximately R_π. However the meausured value of R_{OUT} also seems constant as I_L decreases and this indicates that in Eqn. 4, R_B+R_π is approximately R_B. Since the *rr* is large, then input voltage variations are greatly attenuated. However, the presence of a nonzero output impedance causes changes in the output voltage with load. Since the output impedance specs are more critical, we will trade off low current rr_{LF} in favor of satisfying $Z_{OUT\,LF}$.

Suppose we let β = 50 then $R_\pi = \beta/g_M$ = 125Ω for a current of 10mA. Furthermore, if $R_B = R_\pi$ for this minimum current then R_B will dominate for higher current levels. Thus let R_B = 125Ω. We can now solve Eqn. 2 for A_P. For a DC output voltage of 10, $1+(R_2/R_1)$ = 8. Thus

$$A_P \approx (3055)(8)(125)/(152.75)(50) = 400.$$

Z_{OUT} has a measured zero at about 1.25kHz. Since a pole of A_P is a zero of Z_{OUT} as seen in Eqn. 3, let $1/(2\pi R_P C_{PZ})$ = 1.25kHz. Let R_P = 100Ω then C_{PZ} = 1.27μF. The pole of Z_{OUT} is at high frequencies and we, as yet, do not have a formula for the high frequency behavior. All that we can say is that $1/(2\pi R_Z C_{PZ}) >>$ 1.25kHz and thus $R_Z << R_P$. For this first pass let $R_Z = R_P \div 10{,}000$ = 0.01Ω. The *rr* has a change in magnitude of its slope around 200kHz. Pick this to be the zero of $1/(2\pi R_{BC}C_{BC})$. Let R_{BC} = 1kΩ then C_{BC} = 796pF.

Doing a SPICE AC simulation of the ripple rejection and output impedance, this set of numbers closely resembles the measured responses. Now we can go back to our initial Sspice simulations and use the this set of numeric values to approximate the symbolic results. Sspice has an option which allows the user to set a threshold magnitude to ignore symbolic terms summed with each power of s. Using a 20% approximation we find:

$$rr_{LF} \approx R_{OE}\frac{R_1}{R_2}\frac{\beta A_P}{R_B} \quad (6)$$

$$rr_{HF} \approx 1 + \frac{R_{BC}}{\beta R_L} + \frac{R_1}{R_2}\frac{R_{BC}}{R_B}A_P\frac{R_Z}{R_P} \quad (7)$$

Real poles at

$$\frac{1}{2\pi R_P C_{PZ}} \quad (8)$$

$$\frac{1}{2\pi\beta R_{OE} C_{BC}} \quad (9)$$

Complex conjugate zeros with

$$\omega_O = \sqrt{\frac{1}{R_{BC}C_{BC}}\frac{1}{R_P C_{PZ}}\frac{R_1}{R_2}\frac{\beta A_P}{R_B}\left[R_L \parallel \frac{R_{BC}}{\beta}\right]} \quad (10)$$

$$Q_O = \sqrt{\frac{1}{R_{BC}C_{BC}}R_P C_{PZ}\frac{R_2}{R_1}\frac{R_B}{\beta A_P}\frac{1}{R_L \parallel \frac{R_{BC}}{\beta}}} \quad (11)$$

Similarly we can find the design formulas for Z_{OUT}.

$$Z_{OUT\,LF} \approx \frac{R_2}{R_1}\frac{R_B}{\beta A_P} \quad (12)$$

$$Z_{OUT\,HF} \approx \frac{R_{BC}}{\beta} \parallel R_L \quad (13)$$

Real zeros at

$$\frac{1}{2\pi R_P C_{PZ}} \tag{14}$$

$$\frac{1}{2\pi R_{BC} C_{BC}} \tag{15}$$

Complex conjugate poles with ω_o and Q_o the same as Eqns. 10 and 11.

The simulations of the Z_{OUT} versus frequency matched lab data when Q_O was approximately 0.707. We can use this condition to set Eqn. 11 equal to 0.707. This yields

$$\frac{1}{R_{BC}C_{BC}} = \frac{2}{R_P C_{PZ}} \frac{R_1}{R_2} \frac{\beta A_P}{R_B} [R_L \parallel \frac{R_{BC}}{\beta}] \tag{16}$$

This indicates that the two zeros of Z_{OUT} are very far apart. Thus the frequency where the phase shift of Z_{OUT} is 45° is the frequency of Eqn. 14 and this is the pole of the macromodel op-amp. Next we can use the measurement of the high frequency output impedance of Eqn. 13 to solve for R_{BC}, if we select β. R_B was selected to be equal to R_π at the minimum current level. We now can use Eqn. 12 to solve for A_P and Eqn. 16 to solve for C_{BC}. There are two equations (5 and 9) which contain R_{OE}. Since we traded off matching rr_{LF}, we need to find the pole frequency of rr. This is difficult because of the second order zeros and high frequency pole are similar in value. We can however cancel some of these roots by taking the product of the rr and Z_{OUT}. Doing this we are only left with zero at Eqn. 15 and a pole at Eqn. 9. The zero frequency of Eqn. 15 is much larger than pole frequency of Eqn. 9. Thus the frequency where the sum of the phase angles of rr and Z_{OUT} is -45° is the frequency of Eqn. 9 and we can then find R_{OE}. Using Eqn. 5 and the value of R_{OE}, we now have the SPICE parameter of the pass transistor, V_{AF}. Lastly, use the measurement of rr_{HF} and Eqn. 7 to find R_Z.

Macromodeling the DC Specifications

Some of the dc specifications are already satisfied as a consequence of meeting the ac specifications. The line regulation is the ripple rejection at dc and the load regulation is the measurement of the load forming a voltage divider with the dc output resistance of the regulator.

The adjustment pin current is modeled in Fig. 2 with a current source. The data sheet value of this current is 50μA. Another dc parameter is the dropout voltage. This the minimum difference between the input and output voltages. When this limit is invoked, the pass transistor is at the edge of the active region. In the IC, the Darlington pair causes the dropout voltage to be around 2V. Using a single transistor in the macromodel causes the dropout voltage to be less than a volt. Another potential problem with the macromodel is the fact that dc sources are used in the model. It is possible for these sources to forward bias the base-collector junction of the pass transistor and pump current out of the macromodel's input pin. This, of course, is unacceptable. We can fix both of these problems by placing a diode and resistor in series with the pass transistor. This increases the dropout voltage and blocks current from leaving the input pin. This is shown in Fig. 4 with R_C and D_{BK}.

From this circuit the dropout voltage (DO) is

$$DO = I_C R_C + V_{DBK} + V_{BE} - V_{BC} \tag{17}$$

For small load currents $I_C R_C$ is small and Eqn. 19 is approximately

$$DO \approx V_{DBK} + V_{BE} - V_{BC} \tag{18}$$

Let the SPICE parameter NF be the same for Q_P and D_{BK}, then we can substitute the diode equation into Eqn. 18.

$$DO = 2\,NF\,V_T \ln\frac{I_C}{I_S} - V_T \ln\frac{I_{BC}}{I_S} \tag{19}$$

The value of I_{BC} is small compared to I_C. Let $I_{BC} = I_C/50$ then

$$NF \approx \frac{DO + V_T \ln\dfrac{I_C}{50\,I_S}}{2\,V_T \ln\dfrac{I_C}{I_S}} \tag{20}$$

At higher current levels, the drop across R_C increases. Solving Eqn. 18

$$R_C = \frac{DO - 2\,NF\,V_T \ln\dfrac{I_C}{I_S} + V_T \ln\dfrac{I_C}{50\,I_S}}{I_C} \tag{21}$$

Another dc parameter is the short circuit current. Under these conditions the pass transistor is in the active region. One way to limit the output current is to limit the base current by a factor of β. This can be done by forcing a voltage across the base resistor in Fig. 2. This structure using D_{SC} and E_{SC} is shown in Fig. 4 where R_B is split. This is done to prevent the controlled source from seeing a low impedance path.

If V_{DSC} and V_{BE} are approximately equal, then $E_{SC} = I_B R_{B2}$. Using the large signal model for Q_P we have that

$$I_C = \beta I_B + \beta I_B \frac{V_{CB}}{V_{AF}} \tag{22}$$

Solving partially for I_B

$$I_B = \frac{I_C}{\beta} - I_B \frac{V_{CB}}{V_{AF}} \tag{23}$$

Let the short circuit current be designated as I_{SC} and under these conditions this is the value of I_C. Therefore

$$\begin{aligned} E_{SC} = I_B R_{B2} &= \frac{I_{SC}}{\beta} R_{B2} - I_B R_{B2} \frac{V_{CB}}{V_{AF}} \\ &= I_{SC} \frac{R_{B2}}{\beta} - V_{6,5} \frac{V_{13,5}}{V_{AF}} \end{aligned} \tag{24}$$

Lastly, there is a foldback current effect. Under these conditions, the short circuit current limit is reduced as the input-output voltage differential (V_1-V_2) increases. We can use the same current limiting scheme if we could express the foldback current in terms of $V_{6,5}$ or $V_{13,5}$. This is shown in Fig. 4 with D_{FB} and E_{FB} this circuit,

$$V_1 - V_2 = I_C R_C + V_{DBK} + V_{BE} + V_{13,5} \quad (25)$$

Since Eqn. 25 has V_1-V_2 in terms of $V_{13,5}$ we can solve for $V_{13,5}$.

$$V_{13,5} = V_1 - V_2 - I_C R_C - V_{DBK} - V_{BE} \quad (26)$$

From the data sheet we see that the foldback current is parabolic in shape. Let the short circuit current be a polynomial of second degree, that is,

$$I_{SC} = K_0 + K_1 V_{13,5} + K_2 V_{13,5}^2 \quad (27)$$

Substituting this into the form of Eqn. 24, we have the foldback voltage source

$$E_{FB} = \frac{R_{B2}}{\beta}[K_0 + K_1 V_{13,5} + K_2 V_{13,5}^2] - V_{6,5}\frac{V_{13,5}}{V_{AF}} \quad (28)$$

Macromodeling the Power-Up Response

In the following section it will be shown that line and load transient responses, like those found in the data sheet, are predictable with the macromodel of Fig. 4 However there is another transient response not predicted with Fig. 4. This is the response of the LM117 to a power-up signal. It has been found experimentally that there are two very different responses. The first is that due to a fast rising input and the second is that due to a slow rising input (rise times greater than 5μsec). A thermal overload protector shuts off the regulator due to a fast rising input with a delay of approximately 150μsec. The slow rising input needs a voltage beyond dropout before the regulator can settle to the regulated voltage. This only occurs on the rising edge of the input and produces an overshoot sawtooth on the regulated output.

In the macromodel, the amplifier is active for all inputs. This cannot be true for the actual chip since some level of voltage is needed to forward bias the junctions. One way to produce this effect is to saturate the amplifier during power-up. Observing the transient response of the amplifier model with SPICE, we see that the capacitor C_{PZ} settles to a low voltage of approximately .3V in steady-state. However during power-up the voltage across this capacitor is quite large. By clamping the capacitor with a diode, we can eliminate the gain of the amplifier during power-up. Since the steady-state voltage level is below a diode drop, then as the output reaches its final value the diode will be cutoff. The room temperature macromodel without thermal protection is shown in Fig. 4.

Simulating the power-up circuit with the model of Fig. 4, one finds that the response is close but not exactly that found in lab. Observing the capacitor voltage during power-up, it was found that the peak regulator output voltage varied as the value of E_P was varied. Since the value of E_P is fixed from our AC model, we could vary E_P as long as we inversely varied E_B so as to maintain a product equal to the previous calculated value.

During power-up E_P is a negative slope ramp. The diode D_{PU} clamps the capacitor at approximately 1.286V. When E_P drops to this level, the capacitor can discharge leaving the diode cutoff. Since R_Z is very small, we can neglect it compared with R_P. Performing a source transformation, we have a current source E_P/R_P feeding R_P in parallel with C_{PZ}. Neglecting the current in R_P, we can calculate the change in voltage across C_{PZ}.

Let the overshoot sawtooth have height above the regulated output of ΔV_{OUT} and time width for this case of ΔX. Also let the steady-state regulated voltage across R_I equal V_{RI}. Then

$$\Delta V_{CPZ} = \frac{1}{C_{PZ}}\int_0^{\Delta X}\frac{1}{R_P}\frac{\Delta V_{RI}}{\Delta t}E_P t\,dt = V_{DPU} - E_P V_{RI}$$

Solving for E_P

$$E_P = \frac{V_{DPU} C_{PZ} R_P}{\frac{\Delta V_{RI}}{\Delta t}\Delta X^2 + V_{RI}}$$

Since

$$\frac{\Delta V_{RI}}{\Delta t} = \frac{\Delta V_{OUT}}{\Delta X}\frac{R_1}{R_1 + R_2}$$

then

$$E_P = \frac{V_{DPU} C_{PZ} R_P}{\Delta V_{OUT}\frac{R_1}{R_1 + R_2}\Delta X + V_{RI} C_{PZ} R_P} \quad (29)$$

We can find the values of V_{DPU} and V_{RI} by using the following equations:

$$V_{DPU} \approx NF\,V_T \ln\frac{1A}{I_S} \quad (30)$$

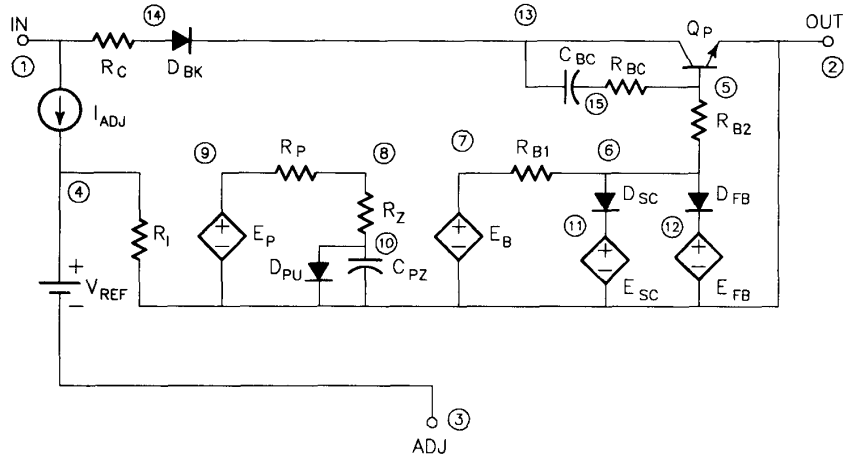
and

$$E_P E_B V_{RI} = \frac{I_C}{\beta}[R_{B1} + R_{B2}] + NF\,V_T \ln\frac{I_C}{I_S}$$

where $I_C = V_{OUT\,DC}/R_L$. Thus

$$V_{RI} = \frac{V_{OUT\,DC}}{R_L}\frac{[R_{B1} + R_{B2}]}{E_P E_B \beta} + \frac{NF\,V_T}{E_P E_B}\ln\frac{V_{OUT\,DC}}{R_L I_S} \quad (31)$$

Use the measured value of $V_{OUT\,DC}$ to solve Eqn. 31. With this solve Eqn. 29 for E_P. Change the values of $E_P E_B$ such that there product remains the same.

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VREF 4 3 1.2782
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CBC 13 15 2.479N
RBC 15 5 247
QP 13 5 2 QLM117HV
RB2 6 5 124
DSC 6 11 DLM117HV
ESC 11 2 POLY(2) (13,5) (6,5) 2.85
+  0 0 0 -70.1M
DFB 6 12 DLM117HV
EFB 12 2 POLY(2) (13,5) (6,5) 3.92
+  -135M 0 1.21M -70.1M
RB1 7 6 1
EB 7 2 8 2 2.56
CPZ 10 2 0.796U
DPU 10 2 DLM117HV
RZ 8 10 .104
RP 9 8 100
EP 9 2 4 2 103.6
RI 2 4 100MEG
.MODEL QLM117HV NPN (IS=30F BF=50
+  VAF=14.27 NF=1.604)
.MODEL DLM117HV D (IS=30F N=1.604)
.ENDS LM117HV
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Figure 4. Room temperature macromodel with no thermal protection

SPICE and Lab Testing of the Macromodel

Applying the design formulas described to additional lab data we find the component parameters listed with Fig. 4.

Simulating the Dropout Voltage, it was found to be 2.226V as compared to lab data of 2.19V. Ripple Rejection is off by about a decade as described previously as a tradeoff. Output Resistance tracks very closely as well as Load Transient Response.

When driving capacitive loads it is important to include the high frequency ESR of the capacitor. This forms a pole-zero cancellation needed for stability.

The following figures show the response of the macromodel using Fig. 3. The lab data in Fig. 5 was entered using the look-up table feature in PSpice's behavior modeling option. PSpice does a point-to-point fit so the lab data appears jagged.

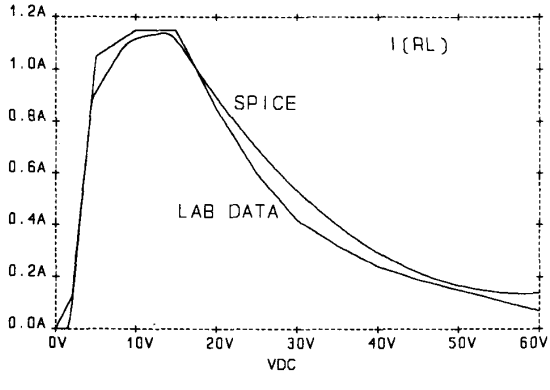

Figure 5. Current Limit vs Input Voltage

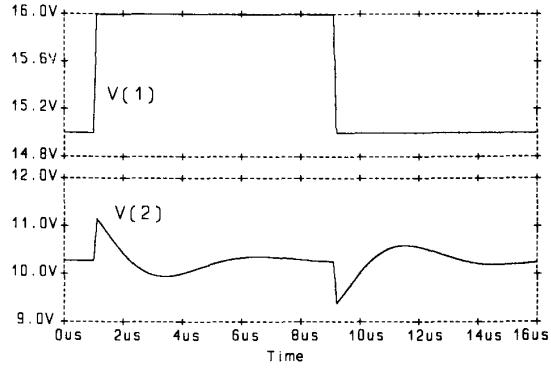

Figure 6. Transient response simulation

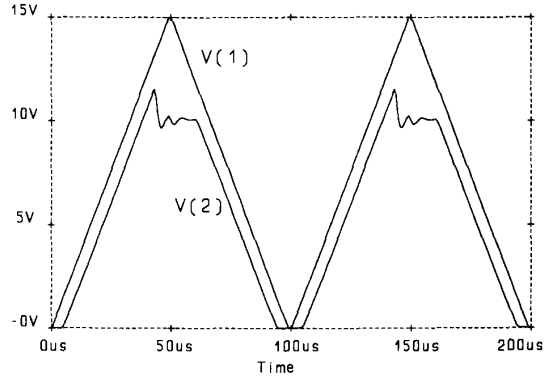

Figure 7. Power-up transient simulation

Acknowledgement

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